

10/05/2022

INVERTER

LAYOUT AND SCHEMATIC USING CADENCE

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**Values found:**

Area = 6.383 m (Length = 4.903m, Width = 1.302m)

EDP = 2.983e-23

Delay(D) = 2.833e-10

Energy(E) = -1.061e-13

**Matrix**

$DATA1 SOURCE='HSPICE' VERSION='O-2018.09-2 linux64' PARAM\_COUNT=0

.TITLE '$example hspice setup file'

trise tfall tavg tdiff

delay iavg energy edp1

t1 t2 t3 t4

i1 i2 energy1 energy2

energysum edp2 temper alter#

1.269e-10 2.833e-10 2.051e-10 1.564e-10

2.833e-10 -8.841e-06 -1.061e-13 3.006e-23

6.001e-09 6.449e-09 6.250e-12 8.971e-10

-1.958e-04 -4.161e-08 -1.052e-13 -4.449e-17

-1.053e-13 2.983e-23 25.0000 1

**Extracted Spice Netlist:**

\* File: INV.pex.netlist

\* Created: Wed Oct 5 08:37:44 2022

\* Program "Calibre xRC"

\* Version "v2013.2\_18.13"

\*

.include "INV.pex.netlist.pex"

.subckt INV GND! OUT VDD! IN

\*

\* IN IN

\* VDD! VDD!

\* OUT OUT

\* GND! GND!

XD0\_noxref N\_GND!\_D0\_noxref\_pos N\_VDD!\_D0\_noxref\_neg DIODENWX AREA=4.78988e-12

+ PERIM=9.382e-06

XMMN0 N\_OUT\_MMN0\_d N\_IN\_MMN0\_g N\_GND!\_MMN0\_s N\_GND!\_D0\_noxref\_pos NFET L=7e-08

+ W=1e-06 AD=3.21e-13 AS=3.09e-13 PD=2.642e-06 PS=2.618e-06 NRD=0.179 NRS=0.161

+ M=1 NF=1 CNR\_SWITCH=1 PCCRIT=0 PAR=1 PTWELL=0 SA=3.09e-07 SB=3.21e-07 SD=0

+ PANW1=5.18e-15 PANW2=3.5e-15 PANW3=3.5e-15 PANW4=3.5e-15 PANW5=3.5e-15

+ PANW6=7e-15 PANW7=1.4e-14 PANW8=1.4e-14 PANW9=1.582e-14 PANW10=0

XMMP0 N\_OUT\_MMP0\_d N\_IN\_MMP0\_g N\_VDD!\_MMP0\_s N\_VDD!\_D0\_noxref\_neg PFET L=7e-08

+ W=2.001e-06 AD=6.42321e-13 AS=6.18309e-13 PD=4.644e-06 PS=4.62e-06

+ NRD=0.0894553 NRS=0.0804598 M=1 NF=1 CNR\_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1

+ SA=3.09e-07 SB=3.21e-07 SD=0 PANW1=0 PANW2=1.82e-15 PANW3=3.5e-15

+ PANW4=3.5e-15 PANW5=3.5e-15 PANW6=1.11052e-13 PANW7=5.0018e-14

+ PANW8=1.6359e-13 PANW9=5.6e-14 PANW10=8.4e-14

\*

.include "INV.pex.netlist.INV.pxi"

\*

.ends

\*

\*

**Layout:**

**Diagram, schematic

Description automatically generated**

**Schematic:**

**Diagram, schematic

Description automatically generated**

**Spice Setup File:**

$example HSPICE setup file

$transistor model

.include "/proj/cad/library/mosis/GF65\_LPe/cmos10lpe\_CDS\_oa\_dl064\_11\_20160415/models/YI-SM00030/Hspice/models/design.inc"

.include "INV.pex.netlist"

.option post runlvl=5

xi GND! OUT VDD! IN inv

vdd VDD! GND! 1.2v

vin IN GND! pwl(1ns 0v 0.75ns 1.2v 1.2ns 1.2v 1.275ns 1.2v 6ns 1.2v 6.075ns 0v 10ns 0v 10.075ns 1.2v 15ns 1.2v 15.075ns 0v 18ns 0v 18.075 1.2v 20ns 1.2v)

cout OUT GND! 70f

$transient analysis

.tr 100ps 20ns

$example of parameter sweep, replace numeric value W of pfet with WP in invlvs.sp

$.tr 100ps 12ns sweep WP 1u 9u 0.5u

**Waveform:**

**Calendar

Description automatically generated with medium confidence**

**Minimum EDP:**

As we already know that Energy and delay are proportional with respect to width of channel to get the **minimum Energy Delay product,** I tried to reduce the width of the channel as much as possible.

Attachments:

Zipfile contains the following documents:

INV.pex.netlist

INV.pex.netlist.INV.pxi

INV.pex.netlist.pex

INV\_Setup.sp

INV\_setup.mt0

INV\_Setup.tr0

Detailed screenshots of the layout